Curriculum Vitae

Dr.SUBHASHINI TATA
Email: tsecegec@gmail.com
Mobile: 9493811529

CARRER OBJECTIVE:

Experienced and dedicated educator with 13 years of teaching, mentoring, and curriculum development experience in Electronics and Communication Engineering. Committed to fostering academic growth and encouraging critical thinking in students through innovative instructional methods and a supportive learning environment. Skilled in leveraging educational technologies and collaborative approaches to maximize student engagement and success. Eager to contribute expertise in Electronics and Communication Engineering to a dynamic academic institution that prioritizes research, student development, and community engagement.

PERSONAL DESCRIPTION:

I consistently achieve results through a problem-solving mindset, swiftly grasp new concepts, and adapt effectively to emerging technologies.

EDUCATIONAL QUALIFICATIONS:

1. 2023 **Ph.D** Awarded a Doctor of Philosophy in Electronics and Communication Engineering by JNTUK, Kakinada, on 30th April 2023. My dissertation, titled *"Design and Analysis of Power Optimized Hybrid Embedded Controller Core Architecture,"* focused on low-power VLSI design.
2. 2011 **M.Tech** Master of Technology (M.Tech) in Digital Electronics & Communication Systems from JNTUK, Kakinada, with 73% marks.
3. 2005 **B.Tech** Bachelor of Technology (Electronics and Communication) from AcharyaNagarjuna University, Guntur with**72.6%**.
4. 2001 **Intermediate** Intermediate (Mathematics, Physics, and Chemistry) from the Board of Intermediate Education, A.P., with 88.8% marks.
5. 1999 **S.S.C** S.S.C from Secondary Board, A.P. with **80%** marks.

PROFESSIONAL EXPERIENCE:

A total of **13** Years in the field of Teaching& Research

- **2012 – Till date** -Assistant Professor in the Department of Electronics and Communication Engineering at Seshadri Rao Gudlavalleru Engineering College, Gudlavalleru.
- **2011-2012-**Assistant Professor in the department of Electronics and Communication Engineering at Sri Vasavi Institute of Engineering & Technology, Nandamuru, Pedana

TEACHING EXPERIENCE:

Courses Taught:

❖ Theory :

Under Graduation:

- Digital Logic & Computer Organization,
- Switching Theory and Logic Design,
- Computer Organization and Microprocessors,
- Microprocessors and Interfacing,
- Microcontrollers and Its Applications,
- VLSI Design,
- Introduction to Embedded systems
- Data Structures
- Signals and Systems ,
- Basic Electronic Devices,
- Embedded Real Time Systems,
- Radar System,

Post-Graduation:

- System Modeling and Simulation,
- Embedded Real Time Operating Systems

❖ Laboratory :

Under Graduation:

- Electronic Devices and Circuits,
- Digital Signal Processing,
- Analog Communication,
- ECAD,
- MPI & MPMC Lab
- Data Structures
- Data Structures using Python

SKILLS & COMPETENCIES:

❖ Technical Skills:

- Assembly language programming of 8086 microprocessor
- Assembly language programming of 8051 Microcontroller
- Data Structures
- Introduction to Programming ('C' –Programming)

RESEARCH INTERESTS & CONTRIBUTIONS:

PUBLICATIONS: 32

➢ Patents Published : 02

1. Patent titled **"Discretization Method for Finding Faults in Analog VLSI Circuits Modelling and Thereof"** was filed on **February 18, 2021**, with Applicant Number **202141006787**. Authored by **M. Kamaraju** and **T. Subhashini**, it was published in the *Journal of Intellectual Property India (IPR)* on **February 26, 2021**, under the Controller General of Patents, Designs, and Trademarks, Department of Industrial Policy and Promotion, Ministry of Commerce and Industry.

URL: https://ipindia.gov.in/writereaddata/Portal/IPOJournal/1_4955_1/Part-1.pdf

2. Patent titled **"Area Delay Power Efficient GSA-Based ALU"** was filed on **November 22, 2021**, with Applicant Number **202141053585A**. Authored by **M. Kamaraju**, **T. Subhashini**, and **K. Babulu**, it was published in the *Journal of Intellectual Property India (IPR)* on **December 3, 2021**, under the Controller General of Patents, Designs, and Trademarks, Department of Industrial Policy and Promotion, Ministry of Commerce and Industry.

➢ Journals : 24

1. Subhashini, T And Kamaraju M, "Design of Power optimized Pipelined 64 – bit Mini Instruction Set Programmable Processor (MISPP)", International Journal of Solid State Technology, Vol.64,Issue 2, Scopus Indexed, IF:0.3, 2021, pp 762-774
URL: http://solidstatetechnology.us/index.php/JSST/article/view/8888.

2. T. Subhashini, M. Kamaraju, K. Babulu, "Power Optimized BCD adder Using Low Power Techniques", Journal of Test Engineering and management, **January-February 2020, ISSN: 0193-4120, pp. 8789 – 8795,** Published by: The Mattingley Publishing Co., Inc.
URL: http://www.testmagzine.biz/index.php/testmagzine/article/view/2228/1990

3. T. Subhashini, M. Kamaraju, K. Babulu, "Low-Power and Fast Adders Using New XOR and XNOR Gates," International Journal of Engineering Research &Technology , ISSN: 0974 – 3154, Volume-12, Number-12, December 2019.
URL: https://www.ripublication.com/irph/ijert19/ijertv12n12_02.pdf

4. T. Subhashini, M. Kamaraju, K. Babulu, "Single Cycle Risc Micro Architecture Processor Using Clock Gating Technique," International Journal of Scientific Technology Research , ISSN: 2277 – 8616, Volume-8, Issue-12, December 2019, pp 2326 – 2334.
URL:http://www.ijstr.org/final-print/dec2019/Single-Cycle-Risc-Micro-Architecture-Processor-Using-Clock-Gating-Technique-.pdf

5. T. Subhashini, M. Kamaraju, K. Babulu, "A New ALU Design using PNS-FCR: Static CMOS Logic for Microprocessors," International Journal of Engineering and Advanced Technology (IJEAT) ISSN: 2249 – 8958, Volume-8, Issue-6S2, August 2019, pp 876-882.
URL:https://www.ijeat.org/wp-content/uploads/papers/v8i6S2/F12150886S219.pdf
DOI: 10.35940/ijeat.F1215.0886S219

6. T.Subhashini, M.Kamaraju,K.Babulu, "A Novel Test Programs for Hybrid RISC Controller," Springer Lecture Notes in Electrical Engineering book series (LNEE,

volume 521), Microelectronics, Electromagnetics and Telecommunications, November 2018, DOI: https://doi.org/10.1007/978-981-13-1906-8_57, Publisher Name: Springer, Singapore, pp 559-565.
URL: https://link.springer.com/chapter/10.1007/978-981-13-1906-8_57
DOI: 10.1007/978-981-13-1906-8_57

7. M. Kamaraju, D. Ramya Krishna, T. Subhashini, "Implementation of A Wallace Tree Approach for Data Aggregation in Wireless Sensor Nodes on ZED board and Send that Aggregated Data to the Sink through WSN Master Development Board(IOT)"International Journal for Research in Engineering Application & Management (IJREAM) ISSN : 2454-9150,IMC18405, Jan 2018, pp 278-287.
URL: https://www.ijream.org/papers/IMC18405.pdf

8. T.Subhashini, M.Kamaraju, K.Babulu, "Programmable core processor using data driven clock gating", International Journal for Modern Trends in Science and Technology(IJMTST), Volume 2 ,Special Issue 1,ISSN:2455-3778,pp:196-203,October,2016 Impact Factor:2.175
URL: http://www.ijmtst.com/documents/NCCEESES34.pdf

9. T.Subhashini, K.Babulu, M.Kamaraju, "Low Power Programmable Processor Core(LPPPC) Architecture Using Clock Gating Technique", Annual Technical Volume of ETDB,Institute of Engineers (India), Theme: Design of Circuits and Systems for Signal,Image and Video Processing, vol. 1, pp. 59-61, 2016.

10. M.Kamaraju, T.Subhashini, "Power efficient convolution using modulo multipliers", International Journal of Applied Engineering and Research, Volume No: 10, Issue No: 21, ISSN: 0973-4562, pp. no: 42581-42587, November, 2015. Peer reviewed,scopus. URL: https://www.ripublication.com/Volume/ijaerv10n21.htm

11. T.Subhashini, M.Kamaraju, "Power Optimized Datapath units of Hybrid Embedded Controller Architecture," International Journal of VLSI Design and Communication Systems, ISSN No: 0976-1357,December 2015, vol.6, No.6, pp: 33-43.
URL: https://www.aircconline.com/vlsics/V6N6/6615vlsi04.pdf
DOI: 10.5121/vlsic.2015.6604

12. S. Anitha, T. Subhashini, Dr. M. Kamaraju, " A Novel Multimodal Medical Image Fusion Approach based on Phase Congruency and Directive Contrast in NSCT Domain", International Journal of Computer Applications, ISBN: 0975-8887, Vol.129,Issue.10, November-2015, pp:30-35.
URL: https://www.ijcaonline.org/archives/volume129/number10/23111-2015907014,
DOI: 10.5120/ijca2015907014

13. T.Subhashini, Y.Srinivasa Rao, K.Rambabu "Design and performance analysis of double precision floating point multiplier using urdhvatriyagbhyam sutra" International Journal of VLSI and Embedded systems, vol.5,issue.10, ISSN:2249-6556,Oct,2014,pp.1313-1317.

14. B.Ruxanayasmin, B.Ananda Krishna, T.Subhashini "Minimization of Power Consumption in Mobile Ad Hoc Networks" International Journal of Computer Networks and Information Security, vol.6,No.2,ISSN(Print)2074-9090,ISSN(online):2074-9104,Jan 2014,pp.38-44.

URL: https://www.mecs-press.org/ijcnis/ijcnis-v6-n2/IJCNIS-V6-N2-6.pdf
DOI: 10.5815/ijcnis.2014.02.06

15. B.Ruxanayasmin, B.Ananda Krishna, T.Subhashini "Implementation of Data Compression Techniques in Mobile Ad hoc Networks" at International Journal of Computer Applications, Volume.80, No.8, October 2013, pp.8-12.Impact factor:0.85
URL: https://research.ijcaonline.org/volume80/number8/pxc3891764.pdf

16. M.Madhurya, B.Ananda Krishna, T.Subhashini "Implementation of Enhanced Security Algorithms in Manets" International Journal of Computer Networks and Information Security, vol.6,No.2,ISSN(Print)2074-9090,ISSN(online):2074-9104,Jan 2014,pp.30-37 Impact factor:N/A
URL: https://www.mecs-press.org/ijcnis/ijcnis-v6-n2/IJCNIS-V6-N2-5.pdf
DOI: 10.5815/ijcnis.2014.02.05

17. N.Madhuri, B.Ananda Krishna, T.Subhashini "Secured Routing Through Multi Stage Authentication in MANETs" at International Journal of Engineering Research & Technology (IJERT), Vol.2, Issue.11, November 2013, ISSN:2278-0181, pp:3509-3515.Impact factor:1.982.
URL:https://www.ijert.org/research/secured-routing-through-multi-stage-authentication-in-manets-IJERTV2IS111086.pdf

18. A.Mallaiah, G.Harish, M.Kamaraju, T.Subhashini, "Implementation of AHB Bus Tracer with dynamic multiresolution for lossless Real time compression" International Journal Of Engineering Science & Advanced Technology (IJESAT) Volume-2, Issue-3, Page no. 445 – 448, ISSN: 2250–3676. Impact factor: 1.14.
URL:https://www.ijesat.org/Volumes/2012_Vol_02_Iss_03/IJESAT_2012_02_0310.pdf

19. A.Mallaiah, M.Ratnakiran, T.subhashini, and Dr. G. N. Swamy "DTT Based Hybrid Embedded Coder For Image Compression Using SPHIT Algorithm" International Journal of Emerging trends in Engineering and development (IJETED), Volume .5, Issue 2, Page No. 740-747, ISSN 2249-6149. Impact factor: 2.87.
URL:https://www.elixirpublishers.com/articles/1354796796_53%20(2012)%2011880-11884.pdf

20. A.Mallaiah, SK.Shabbir, T.Subhashini, and Dr. G. N. Swamy "SPIHT Algorithm with Huffman Encoder for Image Compression and Quality Improvement Using RetinexAlgorithm", International journal of advanced scientific and technical research Volume .4, Issue 2, Page No. 163-170, ISSN 2249-9954. Impact factor: 2.94.
URL:https://www.semanticscholar.org/paper/An-Spiht-Algorithm-With-Huffman-Encoder-For-Image-Mallaiah- Shabbir/2665c64e2fc7208183a6df34ae090132225cb574#citing-papers

21. Subhashini, T And Kamaraju M, Babulu K, "Area and Power optimized D-Flip Flop and Subtractor", Journal of Information Technology in Industry, Vol.9,Issue 1, Web of Science (Emerging Source Citation Indexed), IF:0.3, Year 2021, pp 159-163.
URL: http://www.modern-journals.com/index.php/ijma/article/view/433/355

22. Subhashini, T, Kamaraju M, Babulu.K "Design of Power optimized Pipelined 64 – bit Mini Instruction Set Programmable Processor (MISPP)", International Journal of Solid State Technology, Vol.64,Issue 2, Scopus Indexed, IF:0.3, Year 2021, pp 762-774. URL: http://solidstatetechnology.us/index.php/JSST/article/view/8888

23. T.Subhashini, M.Kamaraju,"Programmable Hybrid Embedded Controller Architecture using Clock Gating Technique", International Journal of Engineering Research in Electronic and Communication Engineering (IJERECE) Vol 3, Issue 1, January 2016.'
URL: https://www.technoarete.org/common_abstract/pdf/IJERECE/v3/i1/4.pdf

24. T. Subhashini, S.V.Brahmam, SkZaheer, V. Raghava, Sk.Vaseem, " Design and Analysis of RISC V Architecture" Journal of Microprocessors and Microcontrollers Research, Vol. 1, Issue 2, 2024
URL: https://matjournals.net/engineering/index.php/JoMMR/article/view/460

➢ IEEE Xplorer/Springer Publications: 04

25. T. Subhashini, M. Kamaraju, and K. Babulu, "FPGA-Based 128-Bit RISC Processor Using Pipelining," Springer Nature Singapore Pte Ltd. 2023, Advances in Signal Processing, Embedded Systems and IoT, Lecture Notes in Electrical Engineering 992, https://link.springer.com/chapter/10.1007/978-981-19-8865-3_2, 2023. pp 11-25

26. T.Subhashini, Dr.M.Kamaraju, Dr.K.Babulu, "Design and Analysis of Multiple Port Memory Architecture for Low Power Applications", Proc. of IEEE 2018 Conference on Signal Processing and Communication Engineering Systems (SPACES), January 2018, pp. 210-214. URL: https://ieeexplore.ieee.org/abstract/document/8316348
DOI: 10.1109/SPACES.2018.8316348

27. T.Subhashini, Dr.M.Kamaraju, Dr.K.Babulu, "A Novel Implementation of Mixed ISA on FPGA", Proc. of IEEE 2017 International Conference on Communication and Signal Processing (ICCSP), December 2017, pp. 0404-0409.
URL: https://ieeexplore.ieee.org/document/8286387
DOI:10.1109/ICCSP.2017.8286387

28. Bala Sindhuri Kandula, Sangeeta Singh, Subhashini Tata, T. Manasaveena, V VijayasriBolisetty and Sadgunakumari V, "Development of a Verilog-Based System for Pattern Detection Using Convolutional Neural Networks,"IEEE 2nd International Conference on Recent Trends in Microelectronics, Automation, Computing and Communications Systems (ICMACC), 2024 (Under publication Process).

➢ Conferences Publications. : 03

29. A.Mallaiah, G.Harish, T.Subhashini, "Design of an on-chip AHB bus tracer for SOC Applications", National Conference on advances in Engineering & Technology SPANDAN 2012, Nagpur 28-29 February-2012.

30. Mallaiah, Sk. Shabbir, T.Subhashini, "A Novel Hybrid HVS based Embedded Image coding Algorithm using DIT and SPIHT", 1st International Conference on AMELIORATIONS in communication and power engineering (ICAP-12), 2-3 March 2012.

31. A.Mallaiah, Sk.Shabbir, T.Subhashini, "An SPIHT Algorithm with Huffman Encoder for Image compression and quality improvement using Retinex Algorithm", 1st international Conference on AMELIORATIONS in communication and power engineering (ICAP-12), 2-3 March 12.

PROJECTS COMPLETED:

The following projects were completed under my supervision:

Under Graduation:

- ✓ Real Time Self Repairable Multiplexer and Full Adder
- ✓ Design and Analysis of RISC-V Processor Architecture.
- ✓ Design of low power linear Feedback Asynchronous circuit using clock gating Approach
- ✓ A High- Speed VLSI Architecture Design of Canonical Huffman Encoder
- ✓ Design and Analysis of an ALU by using GDI Technique
- ✓ Design and Implementation of Low Power 4-Bit ALU Chip by using Ancient Mathematics
- ✓ Design Of Clock Gated Pulse Triggered Intelligent Flip Flop For Low Power High Performance VLSI Synchronous Systems
- ✓ An Approach for Better Traffic Monitoring using Video Segmentation Algorithm for Real Time Applications
- ✓ An Intelligent System for Boarding a Bus

Post Graduation:

- ✓ Design and Analysis of Multiple Port Memory Architecture for Low Power Applications
- ✓ Implementation of Low Power Programmable Core Using Clock and Power Gating Techniques
- ✓ A Novel Multimodal Medical Image Fusion Approach Based on Phase Congruency and Directive Contrast in NSCT Domain
- ✓ Design and Performance Analysis of Double Precision Floating Point Multiplier using UrdhvaTriyagbhyam Sutra

RESEARCHER IDENTITY:

- ORCID ID:0000-0003-2717-9912
- Scopus ID: 57218315272
- Web of Science ID:AAW-8547-2021
- Google Scholar ID:cRC9_AsAAAAJ
- Research gate:https://www.researchgate.net/profile/Subhashini-Tata
- https://vidwan.inflibnet.ac.in/profile/197888

EDITORIAL BOARD MEMBER: 02

- ✓ Journal of Research & Review: Electronics and Communication Engineering (https://matjournals.com/Editorial-Research-&-Review-Electronics-and-Communication-Engineering.html)
- ✓ Journal of Microprocessor and Microcontroller Research (https://matjournals.com/Editorial-Journal-of-Microprocessor-and-Microcontroller-Research.html)

RESEARCH PROJECTS: 02

✓ Co-investigator for the internal R&D project titled *"Design & Development of Intelligent Traffic Control and Traffic Guidance System Using IoT,"* sanctioned with a funding of Rs. 80,000 by GEC authorities in 2019. Duration of the project: 1 year and completed successfully

✓ As a Co-Investigator, contributed to a research proposal titled "*Development of a Virtual Eye System for the Visually Impaired Using Field Programmable Gate Array*," submitted as an internal R&D project to the GEC authorities. The proposal, with a sanctioned budget of Rs. 90,000, was approved for a duration of one year in 2024.

AWARDS AND RECOGNITIONS:

Award: 01

✓ Young Researcher Award 2021 awarded in the year of 2022 by Institute of Researchers, Kerala

NPTEL Courses Completed Successfully: 02

✓ Microprocessors & Microcontrollers Certification with Elite during October 2017
✓ Digital Circuits Certification with Elite during April 2018

TECHNICAL CONTRIBUTIONS:

Guest Lectures Delivered: 02

✓ Delivered a lecture on *"Introduction, working and Applications of General Computing Systems, Microcontrollers and Embedded systems"* during a one-week refresher course on *"Microcontrollers and Embedded Systems,"* held from January 09, 2024, to January 13, 2024, on the fourth day, January 12, 2024.

✓ Delivered a lecture on *"Introduction to Embedded System Design"* during a one-week refresher course on *"Embedded System Design,"* held from July 27, 2020, to August 1, 2020, on the opening day, July 27, 2020.

TECHNICAL PAPERS REVIEWED: 03

✓ Reviewed the technical paper titled *"Design, Verification, and Optimization of the AMBA AHB Lite Protocol"for the* Journal of Microprocessor and Microcontroller Research *in 2024.*.

✓ Reviewed the technical paper titled *"Flood Detection System Using Data Fusion Technique for IoT"* for the Journal of Research & Review: Electronics and Communication Engineering in 2024.

✓ Reviewed the technical paper titled *"Implementation of Multi Account ATM Card using Embedded System "* for the Journal of Microprocessor and Microcontroller Research in 2024.

CURRICULUM DESIGN AND DEVELOPMENT:

- ✓ Member, BoS, ECE, Seshadri Rao Gudlavalleru Engineering College
- ✓ Laboratory Manual Prepared for EDC & ECAD
- ✓ Course Learning Material/Lab Manual prepared for
- Digital Circuits
- Electronic Devices and Circuits
- Signals and Systems
- Data Structures
- Data Structures using Python
- Computer Organization and Microprocessors

PROFESSIONAL AFFILIATIONS:

- ✓ Fellow of Institution of Electronics and Telecommunication Engineers (F-504135)
- ✓ Associate Member of Institution of Engineers (IE) (AM 158546-3)
- ✓ IEEE member (M 99714456)

ADMINISTRATIVE ROLES & CONTRIBUTIONS:

Professional Society Involvement:

- ➢ Elected as Executive Committee member of IETE Vijayawada Centre for the years 2024-2025 & 2025-2026
- ➢ Nominated as CHAIRPERSON, SAHAYA Foundation women's cell (2019-2021)

OTHER RESPONSIBILITIES:

College Level

- ✓ Member : Program Organization Committee, GECFEST'15,16, 17,18,19
- ✓ Member : Discipline Committee, GECFEST'13
- ✓ Coordinator, Techno light (GEC College News Letter)
- ✓ Member : Student MahilaMitra Committee (2019)
- ✓ Member : Grievances Cell

Department Level

- ✓ Member: NBA Criteria IV(2012-13)
- ✓ Member: NBA Criteria V(2015-16)
- ✓ Member: NBA Criteria V(2019-20)
- ✓ Editor: E-Look Department News Letter
- ✓ Advisor: IE Student Chapter (2015-2016)
- ✓ II B.Tech Class Incharge : 2014-2015
- ✓ II B.Tech Class Incharge : 2015-2016
- ✓ Member-VLSI & Embedded System Research Group
- ✓ III B.Tech academic Coordinator
- ✓ Faculty Development Programs coordinator
- ✓ IV B.Tech Exams coordinator

PROFESSIONAL DEVELOPMENT:

➢ Workshops /Conferences /Seminars Organized :

✓ Organized a workshop on **"Image Processing Applications Using MATLAB"** in collaboration with the Institution of Engineers (ISF) and the Department of ECE, Gudlavalleru Engineering College, held at Gudlavalleru on **October 12–13, 2015**.

✓ Organized a workshop on **"Emerging Technology: Internet of Things"** in collaboration with the Institution of Engineers (IE) and the Department of ECE, Gudlavalleru Engineering College, held at Gudlavalleru on **September 21–22, 2015**.

✓ Organized a guest lecture on **"ALIEN VISION: Exploring the Electromagnetic Spectrum with Imaging Technology"** in collaboration with the Institution of Engineers (IE) and the Department of ECE, Gudlavalleru Engineering College, held at Gudlavalleru on **September 15, 2015**.

✓ Organized a guest lecture on **"Future Development of Product/Solution"** in collaboration with ECSAt and the Department of ECE, Gudlavalleru Engineering College, held at Gudlavalleru on **September 5, 2015**.

✓ Organized a guest lecture on **"Detection and Estimation in SONAR Signal Processing"**, conducted by the Department of ECE, Gudlavalleru Engineering College, held at Gudlavalleru on **August 1, 2015**.

✓ A one-week international online Knowledge Development Programme on **"Challenges and Advancements in the Design of IoT, Embedded, and VLSI Systems: A Researcher's View (CADIEVR-2020)"**, organized by the Department of Electronics and Communication Engineering, Gudlavalleru Engineering College, Gudlavalleru, held from **June 8 to 13, 2020**, where I served as the convenor.

➢ Workshops /Conferences /Seminars Attended:

✓ Attended a One week Refresher course on **"Transmission lines and Waveguides"**, organized by Department of Electronics and Communication Engineering, Seshadri Rao Gudlavalleru Engineering College, Gudlavalleru during 29th January 2024 to 02nd February 2024.

✓ Attended a One week Refresher course on **"Microcontrollers and Embedded Systems"**, organized by Department of Electronics and Communication Engineering, Seshadri Rao Gudlavalleru Engineering College, Gudlavalleru during 09th January 2024 to 13th January 2024.

✓ Attended a one week National Level Faculty Development Program on **"Applications of Computer Vision using Deep Learning"**, organized by Department of Electronics and Communication Engineering, Seshadri Rao Gudlavalleru Engineering College, Gudlavalleru during 20th February 2023 to 25th February 2023.

✓ Attended a Faculty Development Programme on **"Insights of NEP 2020 and Strategies for its Implementation"**, organized by Academic Strengthening and Advancement Cell, Seshadri Rao Gudlavalleru Engineering College, Gudlavalleru on 12th June 2022.

✓ Attended a One Week Online Faculty Development Program on **"Trends and Challenges in Advanced VLSI System Design"**, organized by Department of ECE, SRKR Engineering College (A) during 21st to 26th February 2022.

✓ Attended a One Week Online Faculty Development Program on **"Trends and Challenges in Advanced VLSI System Design"**, organized by Department of Electronics and Communication Engineering, Vardhaman College of Engineering, Shamshabad, Hyderabad during 27th to 31st December 2021.

✓ Attended a AICTE-ISTE sponsored one week online induction programme on **"Millimeter wave frequencies"**, organized by Department of Electronics and Communication Engineering, Gudlavalleru Engineering College, Gudlavalleru during 17th to 24th August 2021.

✓ Attended a One Week Online STTP on **"Mixed Signal Design"**, organized by Department of Electronics and Communication Engineering, Vasireddy Venkatadri Institute of Technology, Guntur during 26th to 31st October 2020.

✓ Attended Online Three Day Higher Education Conclaveon **"Higher Education Conclave"**, organized by IEEE Guntur Sub Section in collaboration with IEEE Education Society Chapter, Hyderabad Section during 15th to 17th October 2020.

✓ Attended National Level Online Faculty Development Program on **"Recent Advances in VLSI & Embedded Systems (RAVDES-2020)"**, organized by Micro Electronics Research Group (MERG), Department of Electronic and Communication Engineering, Koneru Laksmaiah Education Foundation (KL Deemed to be University) during 14th to 19th September 2020.

✓ Attended AICTE Sponsored Online Short term Training Programme on **"Block Chain Architecture Design and Use Cases, (Smart Contracts with Ethereum Solidity) Phase-III"**, organized by Department of Electronics and Communication Engineering, Gudlavalleru Engineering College, Gudlavalleru during 24th to 29th August 2020.

✓ Attended AICTE Sponsored Online Short term Training Programme on **"Block Chain Architecture Design and Use Cases, (Decentralized Network Synchronization) Phase-II"**, organized by Department of Electronics and Communication Engineering, Gudlavalleru Engineering College, Gudlavalleru during 17th to 22nd August 2020.

✓ Attended AICTE Sponsored Online Short term Training Programme on **"Block Chain Architecture Design and Use Cases, Phase-I"**, organized by Department of Electronics and Communication Engineering, Gudlavalleru Engineering College, Gudlavalleru during 10th to 15th August 2020.

✓ Attended One Week Refresher Course on **"Embedded System Design"**, organized by Department of Electronics and Communication Engineering, Gudlavalleru Engineering College, Gudlavalleru during 27th July to 1st August 2020.

✓ Presented a paper titled **"Power Optimized BCD Adder Using Low Power Techniques"** at the **International Conference on Computing, Communication, Electrical, and Electronics Engineering (ICCCEEE 2020)**, held at G. Pulla Reddy Engineering College, Kurnool, on January 10–11, 2020.

✓ Attended a One Week International Online Knowledge Development Program on **"Challenges and Advancements in the Design of IoT, Embedded and VLSI Systems: A**

Researchers View", organized by Department of Electronics and Communication Engineering, Gudlavalleru Engineering College, Gudlavalleru during 8th to 13th June 2020.

✓ Attended a One Week National Level Online Faculty Development Program on **"Research Challenges and Emerging Trends In Electronics and Communication Engineering (RCEECE-2020)"**, organized by Department of Electronics and Communication Engineering, Ramachandra College of Engineering, Eluru during 27th May to 1st June 2020.

✓ Attended a Five Days Online Certificaion Program on **"Industrial IOT"**, organized by Apply Volt during 19th to 23rd May 2020.

✓ Attended a Online FDP on **"Internet Of Things"**, organized by APSSDC during 18th May to 30th May 2020.

✓ A Two Day Training Programme on **"Design and Development of Digital Circuits using VLSI Tools"** organized by the Department of Electronics and Communication Engineering, Gudlavalleru Engineering College, Gudlavalleru, held from 6th December 2018 to 7th December 2018**.**

✓ A one-week Faculty Development Programme (FDP) on **"Communication and Signal Processing"** organized by the Department of Electronics and Communication Engineering, Gudlavalleru Engineering College, Gudlavalleru, held from October 29 to November 3, 2018**.**

✓ The **33rd National Convention of Electronics and Telecommunication Engineers** and National Seminar on **"Recent Advances in IoT"**, organized by The Institution of Engineers (India), Telangana State Centre, in association with the Department of Electronics and Communication Engineering, Spoorthy Engineering College, Hyderabad, held from November 29 to 30, 2017**.**

✓ A two-day Faculty Training Programme on **"Advances in VLSI Design and Embedded Systems"**, organized by the Department of Electronics and Communication Engineering, Gudlavalleru Engineering College, held from November 6 to 7, 2017**.**

✓ A one-week National Level Faculty Development Programme (FDP) on **"Signal and Image Processing using LabVIEW"**, organized by the Signal Processing Research Group of the Department of Electronics and Communication Engineering, Gudlavalleru Engineering College, in association with NI Systems Pvt. Ltd., held from November 13 to 18, 2017**.**

✓ A two-day Faculty Training Programme on **"Mentor Graphics Tools"**, organized by the Department of Electronics and Communication Engineering, Gudlavalleru Engineering College, held from **August 31 to September 1, 2017**.

✓ A two-day National Level Workshop on **"Advances in Electronics and Communication Engineering"**, organized by JNTUK, Kakinada, held from **August 26 to 27, 2017**.

✓ A two-week Faculty Development Programme on **Entrepreneurship**, organized by the Department of MBA, Gudlavalleru Engineering College, Gudlavalleru, held from **February 6 to 21, 2017**.

✓ A two-week ISTE STTP on **"CMOS, Mixed Signal, and Radio Frequency VLSI Design"**, conducted by the Indian Institute of Technology Kharagpur under the National Mission on Education through ICT (MHRD), held from **January 30 to February 4, 2017**.

✓ A one-week Faculty Development Program on **"Hands-on Experience in Signal Processing Applications"**, organized by the Department of Electronics and Communication, Gudlavalleru Engineering College, Gudlavalleru, held from **November 7 to 12, 2016**.

✓ Participated in the **National Convention and National Seminar** on **"Intelligent Systems for a More Connected World: Internet of Things"**, organized by The Institution of Engineers, Andhra Pradesh State Center, held on **October 24–25, 2016**.

✓ A one-week National Workshop on **"Recent Advancements in VLSI Technology and Design Using EDA Tools (VLSITP-2016)"**, organized by the Department of Electronics and Communication, UCEK (A), JNTUK, Kakinada, sponsored by TEQIP-II, held from **July 20 to 24, 2016**.

✓ A two-week Audit Course on **"Research Methodologies"**, organized by the Department of Electronics and Communication, UCEK (A), JNTUK, Kakinada, held from **May 1 to 15, 2016**

✓ A two-week Credit Course on **"EDA Tools"**, organized by the Department of Electronics and Communication, UCEK (A), JNTUK, Kakinada, held from **May 1 to 15, 2016**.

✓ A three-day workshop on **"Swarm Intelligence Techniques: Applications to Signal Processing"**, organized by the Department of Electronics and Communication, Gudlavalleru Engineering College, Gudlavalleru, held from **February 5 to 7, 2016**.

✓ A three-day workshop on **"Overview of Latest Telecom Technologies"**, organized by BSNL Krishna SSA, held from **January 11 to 13, 2016**.

✓ A three-day workshop on **"Swarm Intelligence Techniques: Applications to Signal Processing"**, organized by the Department of Electronics and Communication, Gudlavalleru Engineering College, Gudlavalleru, held from **February 5 to 7, 2016**.

✓ A one-week Faculty Development Program (FDP) on **"Development of Wireless Sensor Network Simulator (NS2) – Hands-on Experience"**, organized by the Communication Research Group, Department of Electronics and Communication, Gudlavalleru Engineering College, Gudlavalleru, in association with Vertex Soft, Hyderabad, held from **December 1 to 5, 2015**.

✓ A one-week Refresher Course on **"Microprocessors and Microcontrollers"**, organized by the Department of Electronics and Communication, Gudlavalleru Engineering College, Gudlavalleru, held from **November 17 to 21, 2015**.

✓ A two-day workshop on **"Image Processing Applications Using MATLAB"**, organized by the Department of Electronics and Communication, Gudlavalleru Engineering College, Gudlavalleru, held from **October 12 to 13, 2015**.

✓ A two-day All India workshop on **"Emerging Techniques in VLSI Architecture Design for Real-Time Environment"**, organized by the Department of Electronics and Communication Engineering, PACE Institute of Technology & Sciences, Ongole, held from **October 9 to 10, 2015**.

✓ A two-day workshop on **"Real-Time Signal & Image Processing Using Xilinx Vivado and Zynq-7000 SOC"**, organized by the Department of Electronics and Communication Engineering, SRK Institute of Technology, Vijayawada, in collaboration with CoreEL Technologies, Bangalore, held on **September 11–12, 2015**.

✓ A two-day workshop on **"All India Seminar on Agricultural, Horticultural – Unmanned Aerial Vehicles in Micro Farming"**, organized by the IE(I), Vijayawada Local Centre, in association with Sri Vishnu College of Engineering, Bhimavaram, held on **March 26–27, 2015**.

✓ A one-day workshop on **"Research and Development Facilitation"**, organized by the IE(I), Vijayawada Local Centre, Vijayawada, held on **March 29, 2015**.

✓ Attended a one-day workshop on **"Research in Energy Management"** at Vijayawada, conducted by the Institution of Engineers (India), on **March 29, 2015**.

✓ A one-day workshop on **"Ultra Low Power Communication Using CC430 Microcontroller: Hands-on Experience"**, organized by the ECE Department of Gudlavalleru Engineering College, held on **February 7, 2015**.

✓ A four-day coursework on **"Research Methodology"**, organized by KL University, Vaddeswaram, held from **January 3 to 6, 2015**.

✓ A one-day seminar on **"Research in Signal and Image Processing on FPGAs and Embedded Platforms"**, organized by the IE(I), Vijayawada Local Centre, Vijayawada, held on **November 22, 2014**.

✓ A one-day workshop on **"Speech Processing: Current Challenges and Hands-on Experience"**, organized by the ECE Department of Gudlavalleru Engineering College, held on **August 23, 2014**.

✓ A three-day national-level workshop on **"Theory & Applications of Intelligent Signal Processing"**, organized by the ECE Department of Gudlavalleru Engineering College, Gudlavalleru, held from **February 28 to March 2, 2014**.

✓ A two-day workshop on **"Issues in Integrated Circuits (ICs) Design"**, held on **December 13–14, 2013**, at Gudlavalleru Engineering College.

✓ A two-week refresher course on **"Electronics Devices and Circuits"**, held from **September 23 to 28, 2013**, at Gudlavalleru Engineering College.

✓ A one-week workshop on **"Training Teachers for Excellence"**, conducted by Dr. B. G. Barki, Former Director, NITTTR, Chennai, held from **June 7 to 21, 2013**, at Gudlavalleru Engineering College.

✓ A two-week workshop on **"Analog Electronics"**, conducted by the Indian Institute of Technology Kharagpur, held from **June 4 to 14, 2013**, at Gudlavalleru Engineering College.

✓ A webinar on **"Career Choices in Civil Services"** by Dr. KiranmayiKoppisetti, IRTS, who secured an All India Rank of 573 in UPSC, organized by the Department of Electronics and Communication Engineering, Gudlavalleru Engineering College, on **June 30, 2020**. A total of **185 students** participated.

➢ Webinars Attended:

✓ A webinar on **"Introduction to Radio Frequency Measurements for Cellular and Wireless Communication Systems"**, organized by the Department of Electronics and Communication Engineering, Gudlavalleru Engineering College, on **May 25, 2020**. The resource person was **Dr. Ramakrishna Yellapantula**, Senior Member of Technical Staff, Lite Point Corporation, USA. A total of **85 participants** attended.

✓ Attended a national-level online Faculty Development Program on **"Research Challenges and Emerging Trends in ECE"**, organized by the Department of ECE, Sri Ramachandra College of Engineering, held from **May 7 to June 1, 2020**.

✓ Attended a webinar on **"Impact of COVID in Engineering Education & Way Forward"**, organized by the ISTE Chapter, GEC, on **June 9, 2020**.

PROJECTS COMPLETED DURING MY GRADUATION, POST-GRADUATION & PHD:

➢ PhD/ Research Work:

Title: Design and Analysis of Power Optimized Hybrid Embedded Controller core architecture.

Abstract : The primary objective of this work is to develop a prototype power-optimized Hybrid Embedded Controller (HEC) core architecture designed for an FPGA chip and analyze the power consumption of various components, such as the datapath, control circuits, ALU, etc. A dynamic power management system, incorporating techniques like clock gating, qualified system latches, bus deactivation, and clock error detection, is employed to implement the HEC core, which combines RISC and CISC with a Microcontroller Featured Architecture.

A novel control unit will be designed with the capability to generate clock gating signals during the fetching and execution of instructions. Serving as the core of the Hybrid Embedded Controller, the control unit facilitates the necessary signal interactions for proper data flow and execution of desired functions. Additionally, the clock management system includes clock distribution, ensuring that clock signals are directed to the appropriate modules based on the clock gating signals generated by the control unit.

➢ M.Tech Project:

Title: Post Processing Technique for Speech Enhancement in non-stationaryEnvironments.

Overview: This work introduces a novel and straightforward approach for speech enhancement by integrating two spectral magnitude estimators for both speech and noise. The decision on which estimator to use is based on the implicit maximization of the signal-to-residual spectrum ratio, a metric that has been shown to strongly correlate with both speech quality and intelligibility. The estimator for the spectral magnitude of the noise takes the same form as the speech spectral magnitude estimator. Once the noise's magnitude spectrum is estimated, the speech signal's spectrum can be easily derived. This approach proposes a simple rule to combine both estimators in a way that maximizes the signal-to-

residual spectrum ratio.

- **B.Tech Project:**

Title: Analysis of Bit Error Probability of UWB-TH PPM systems with theMultipleAccessInterference

Overview: The objective of this project is to develop a straightforward and comprehensive expression for calculating the Bit Error Rate (BER) of an Ultra Wide Band Time Hopping (UWBTH) system, which utilizes Pulse Position Modulation (PPM). The Multiple Access Interference (MAI) is represented using the Characteristic Function (CF) technique, coupled with the Gaussian Approximation (GA). The results obtained demonstrate a strong correlation with the actual behavior of the system.

PERSONAL DETAILS:

Name	: Subhashini Tata
Husband Name	: A. E. Srinivasa Rao
Sex	: Female
Marital Status	: Married
Nationality	: Indian
Permanent Address	: **Dr. Subhashini Tata** 21/553-18A, Parasupet, Machilipatnam. Phone:9493811529
Date of Birth	: 19-01-1984.

Declaration

I certify that the information provided above is accurate to the best of my knowledge, and I take full responsibility for its accuracy.

Place: Machilipatnam
Date:

(Dr.SUBHASHINI TATA)